

FIG.1

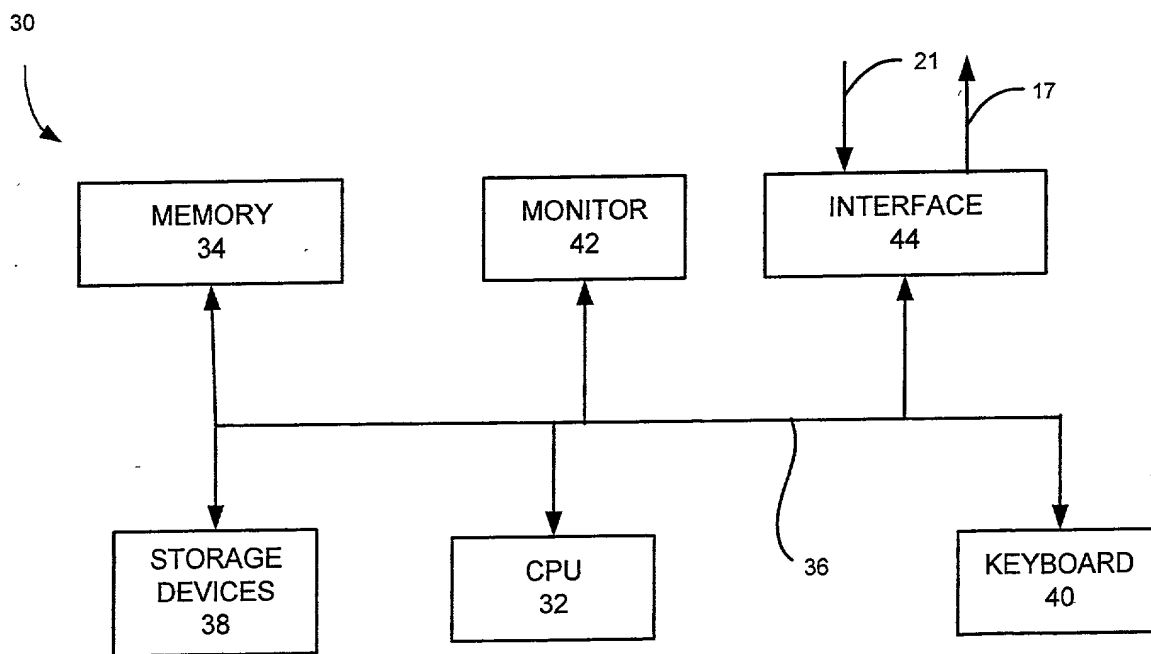
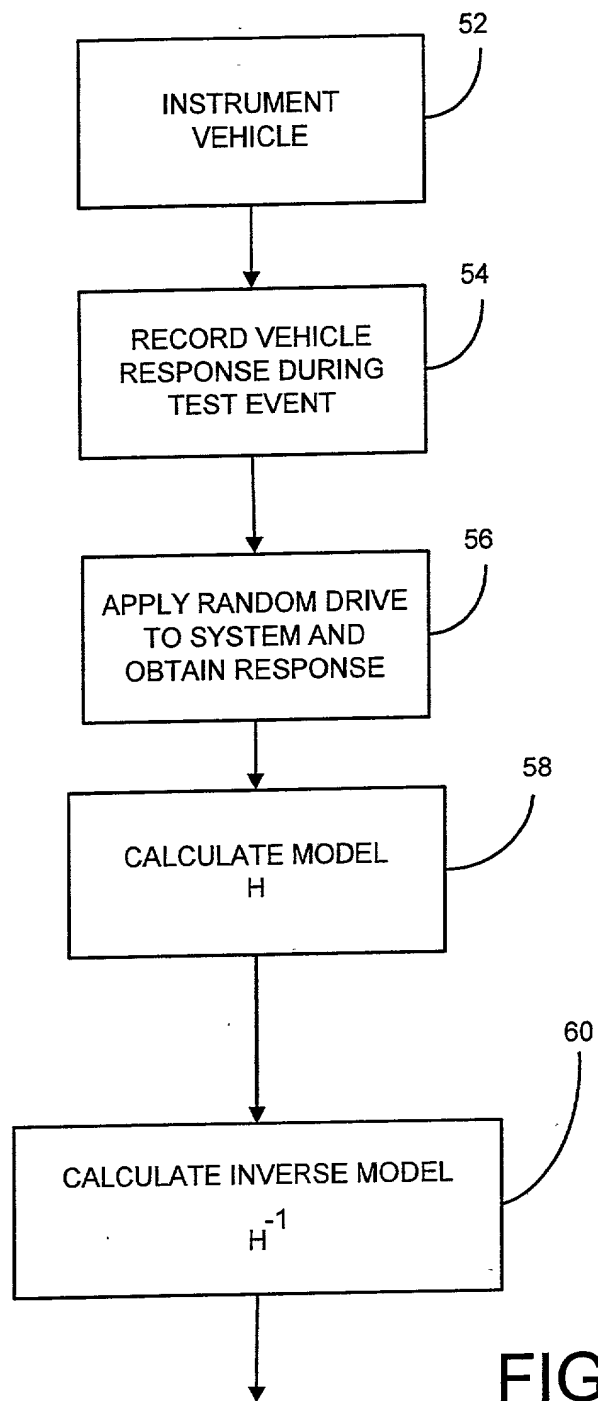


FIG.2



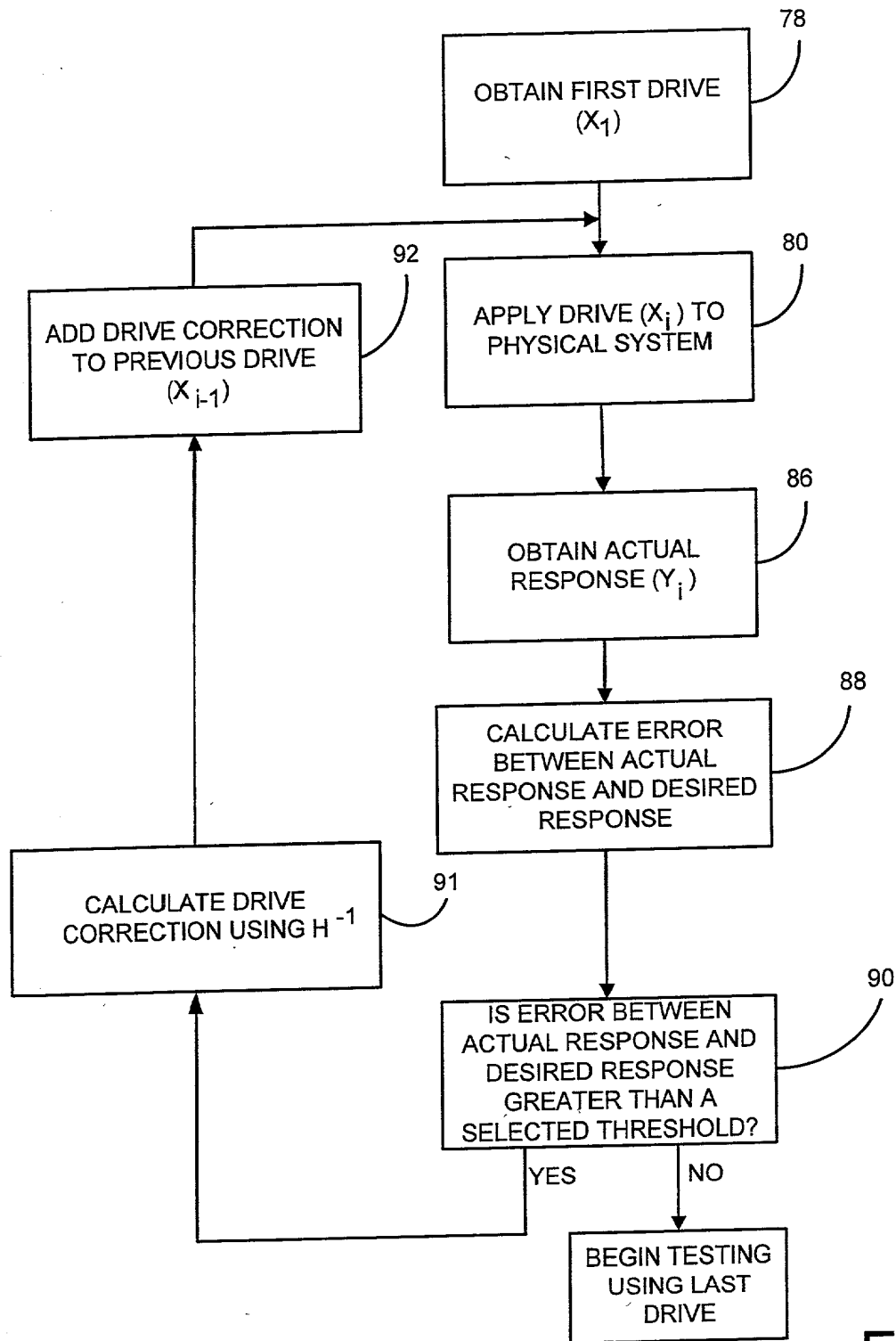


FIG. 3B

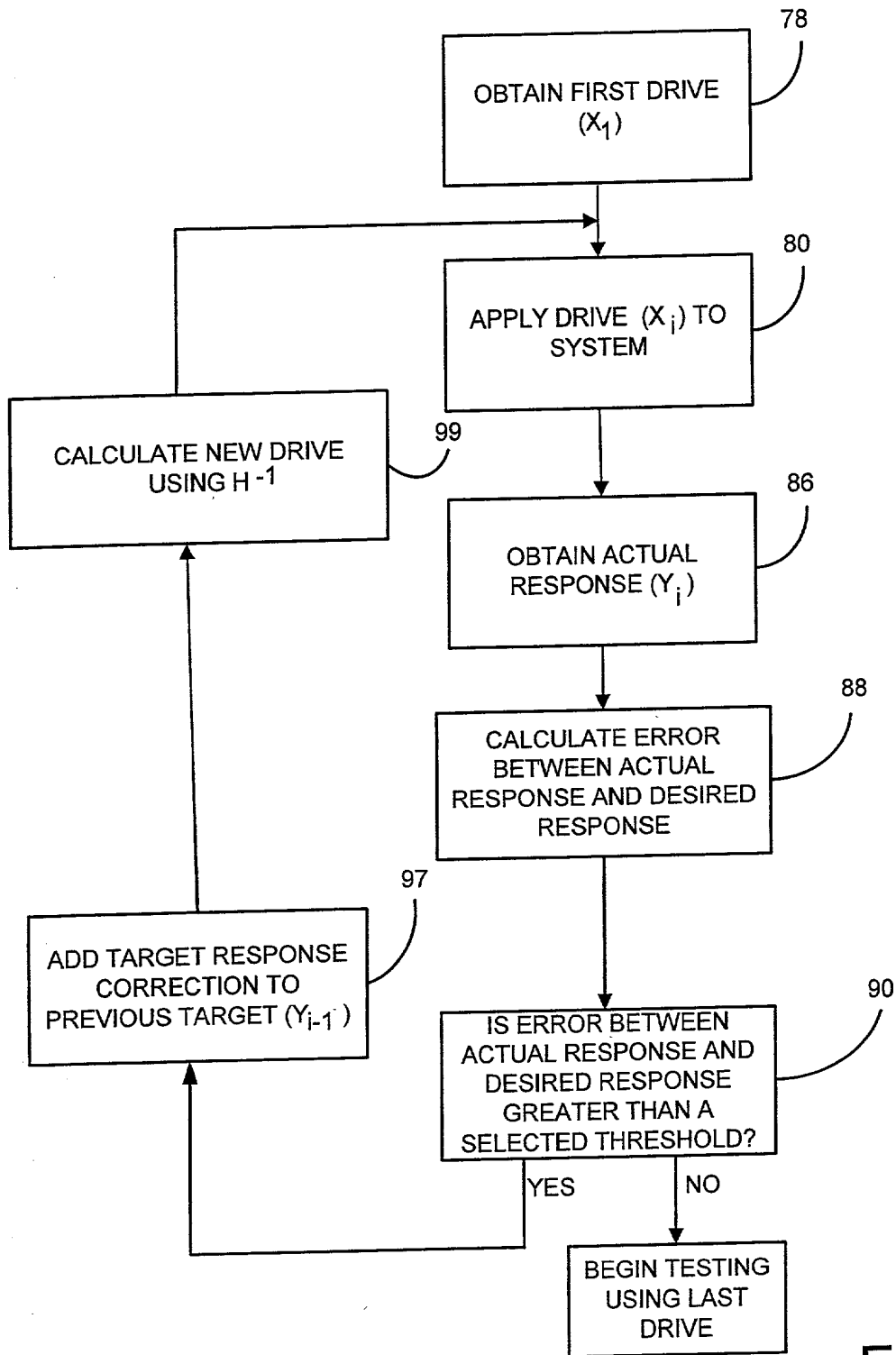


FIG. 3C

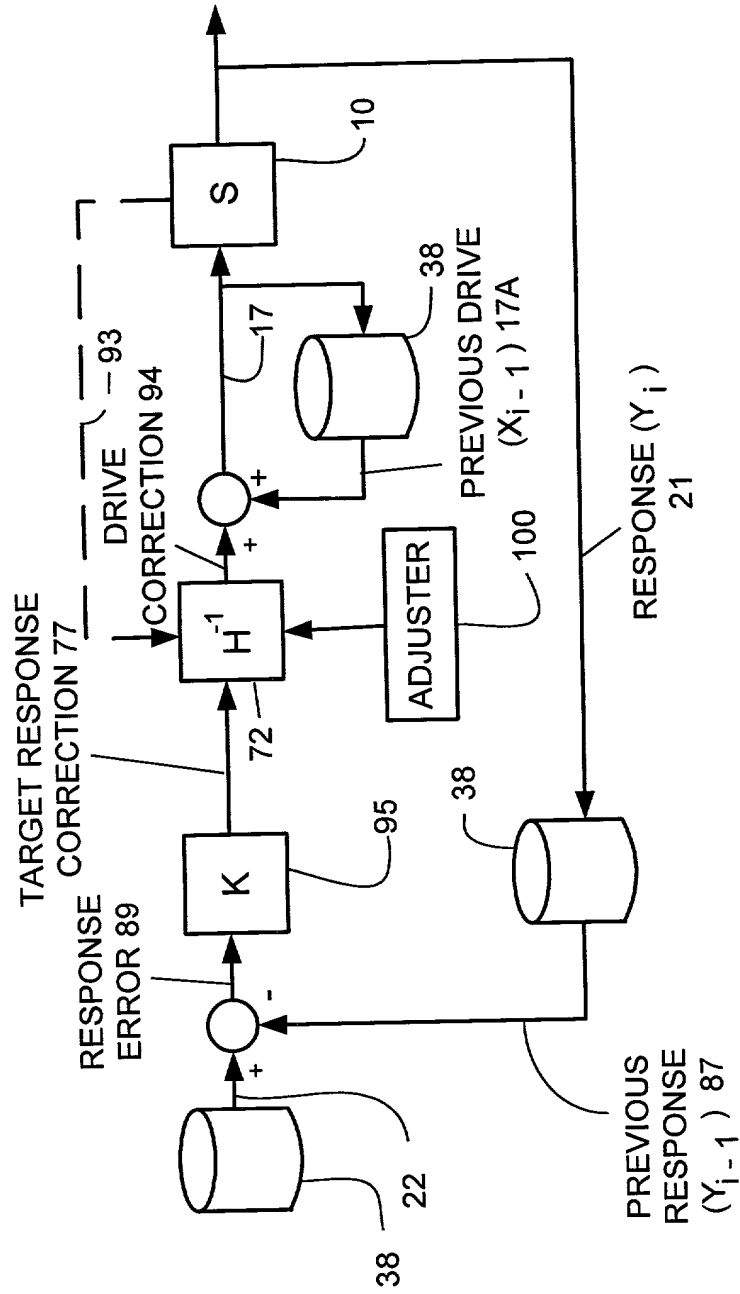


FIG. 4A

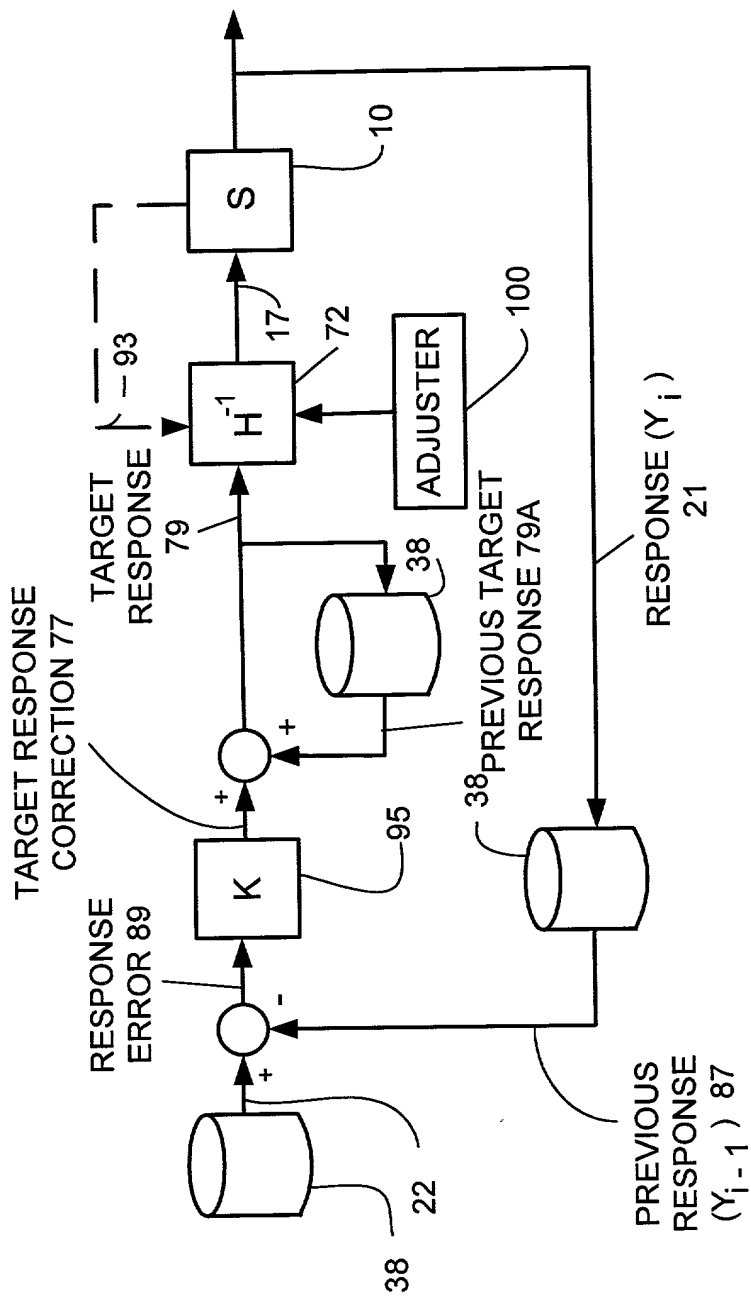


FIG. 4B

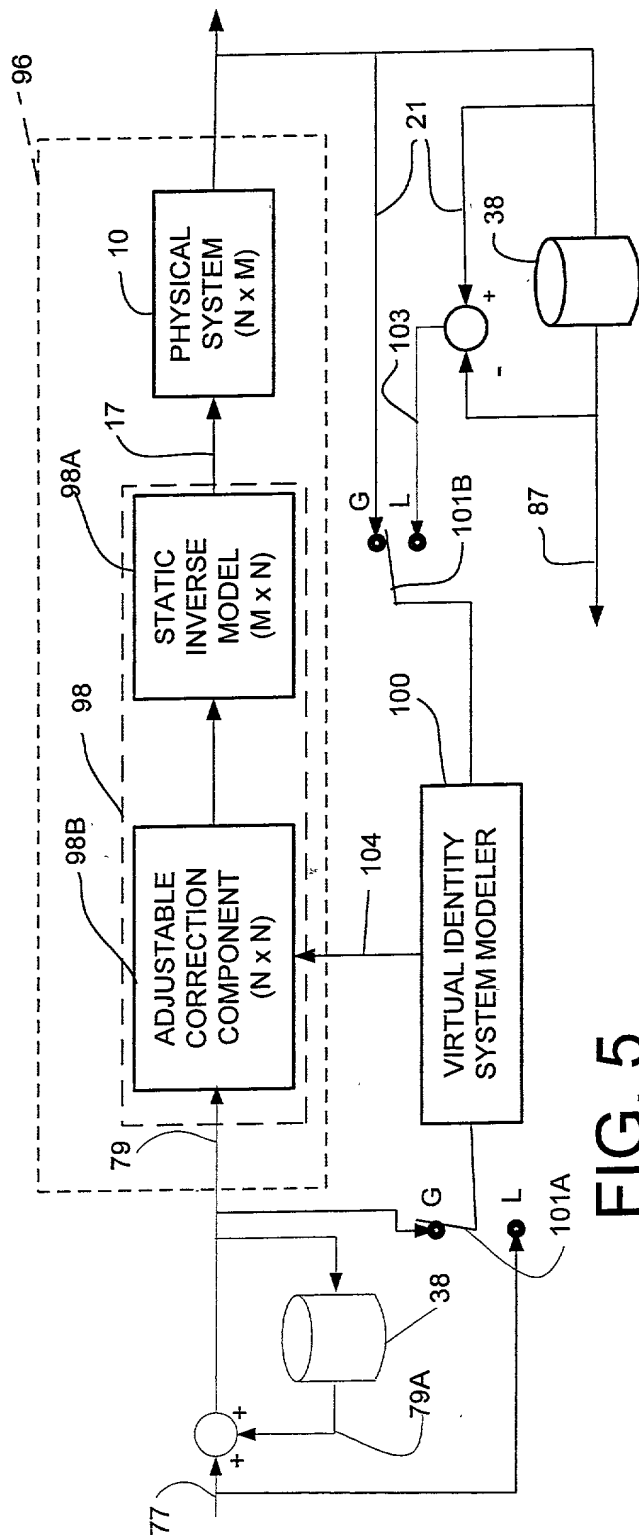


FIG. 5

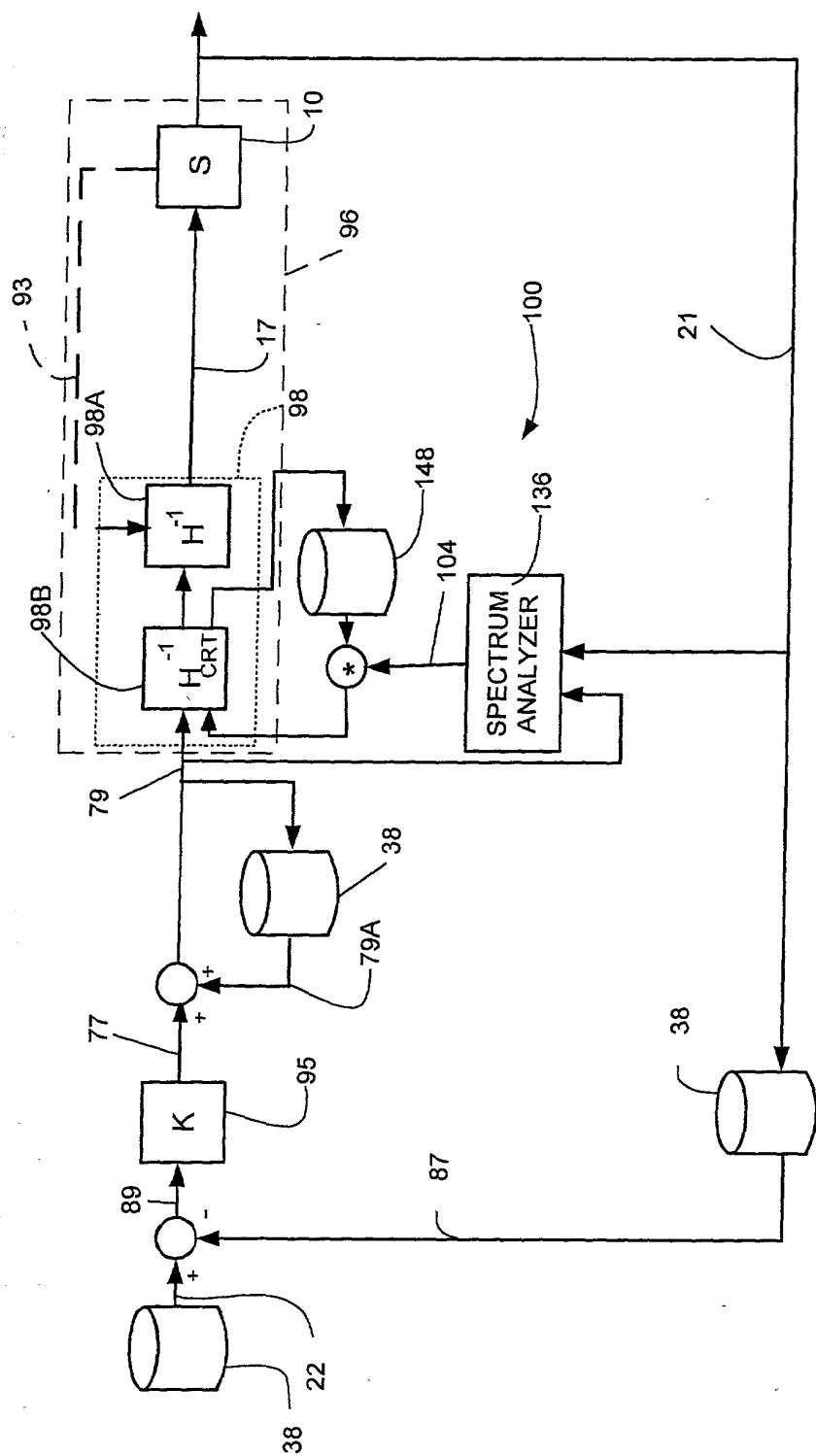


FIG. 6

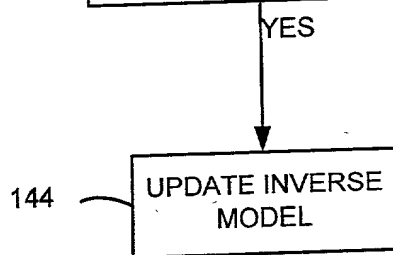
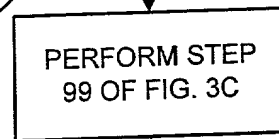
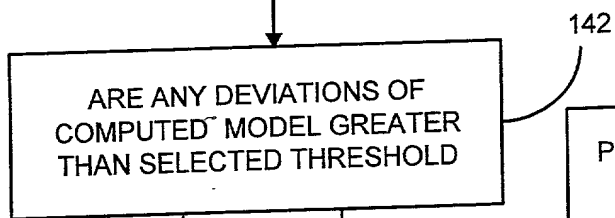
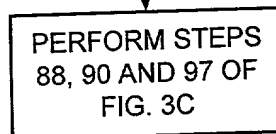
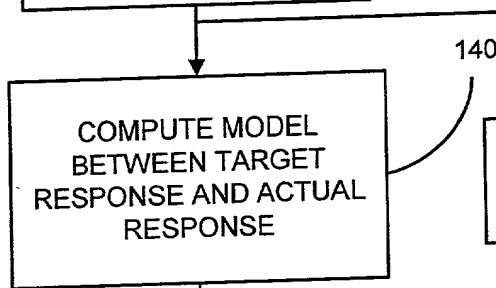
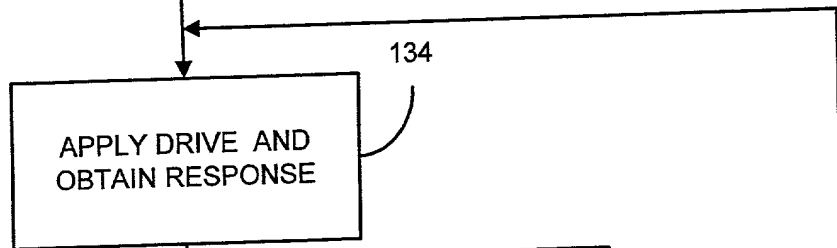
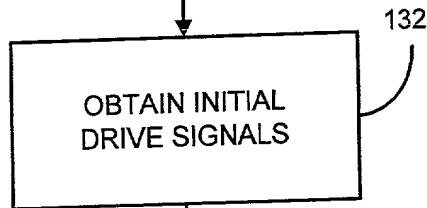
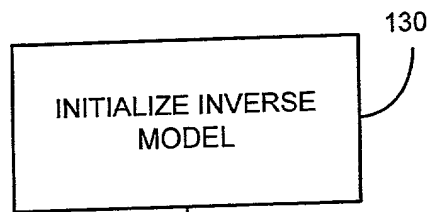
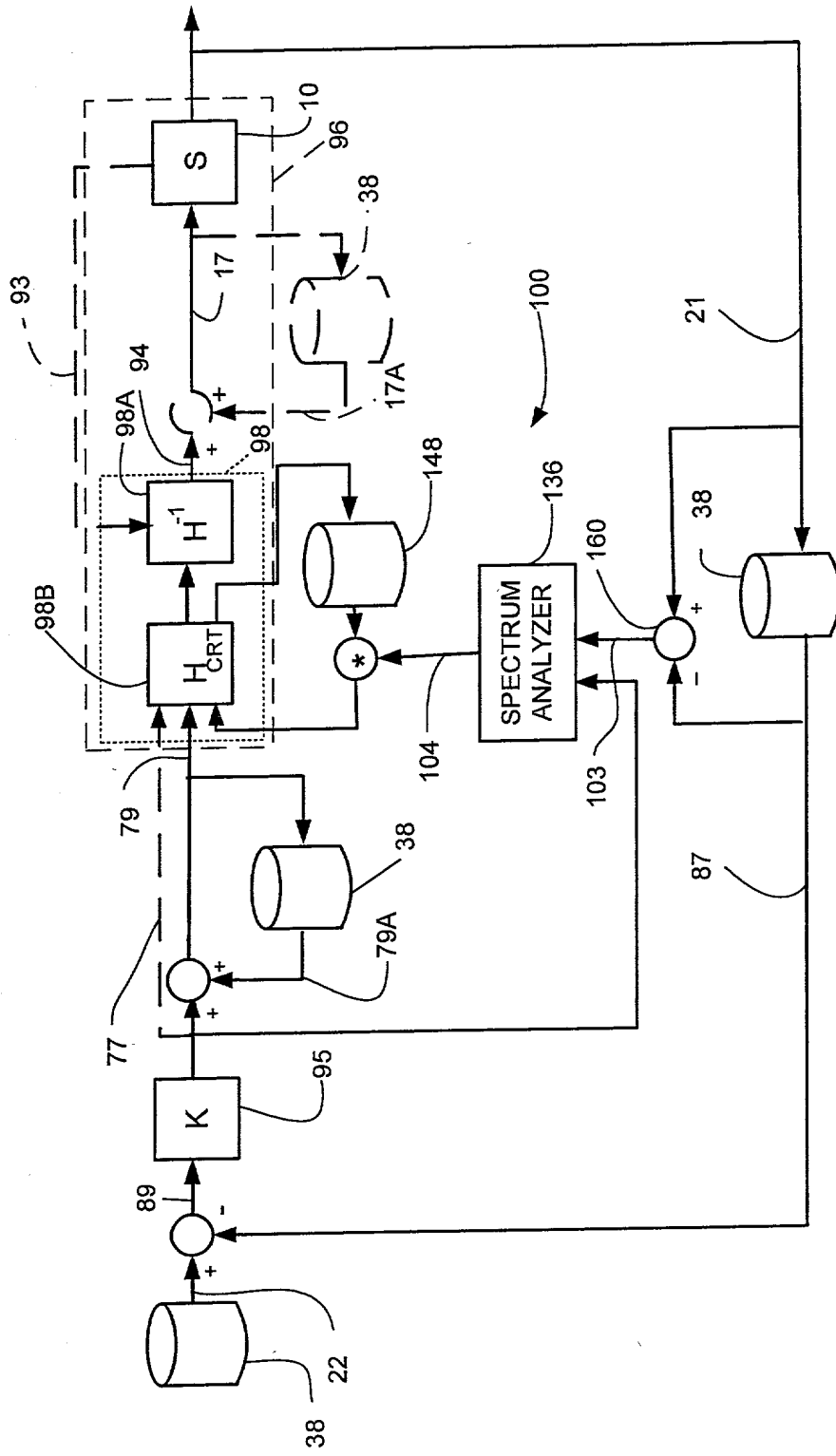
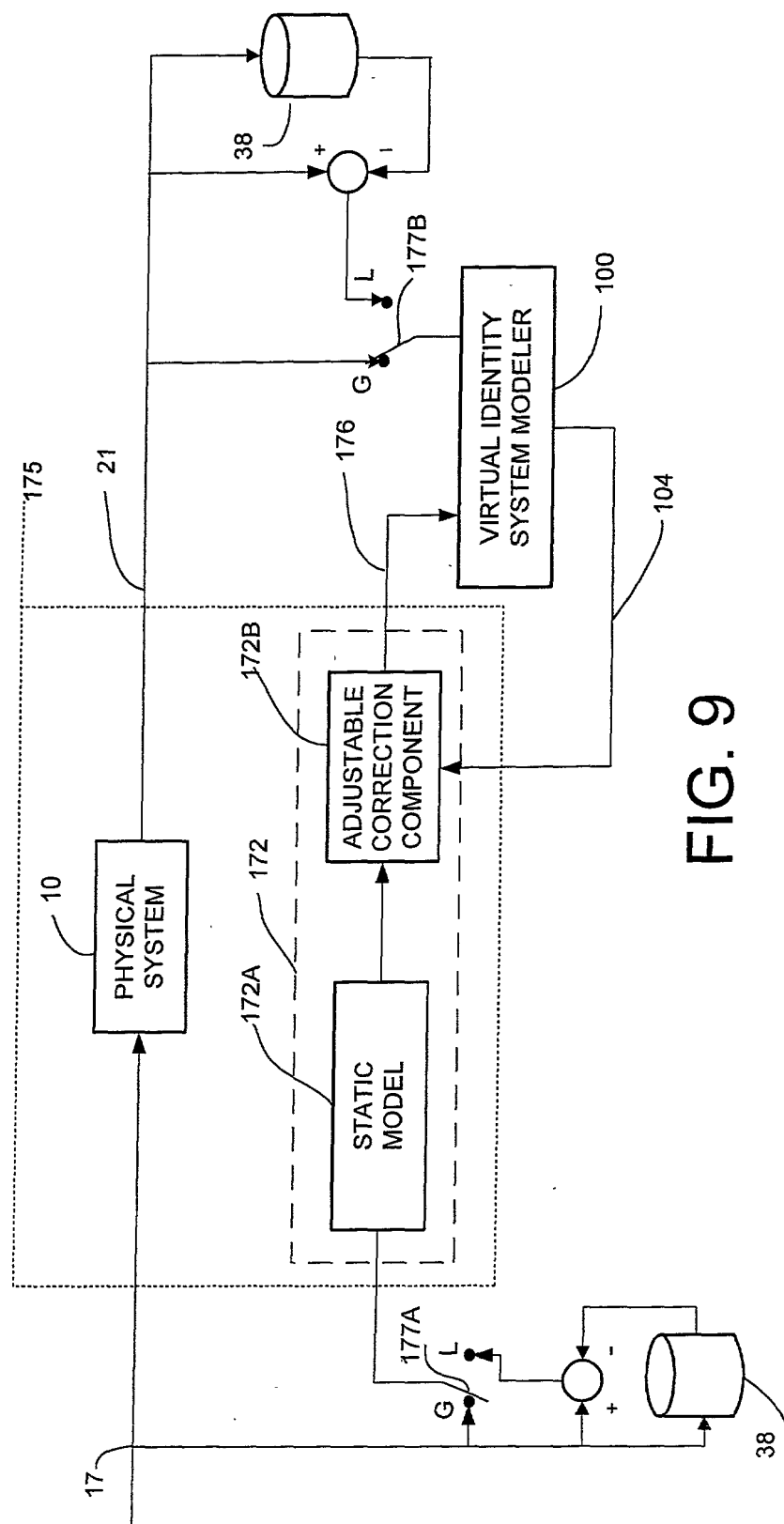


FIG. 7



F/G.8



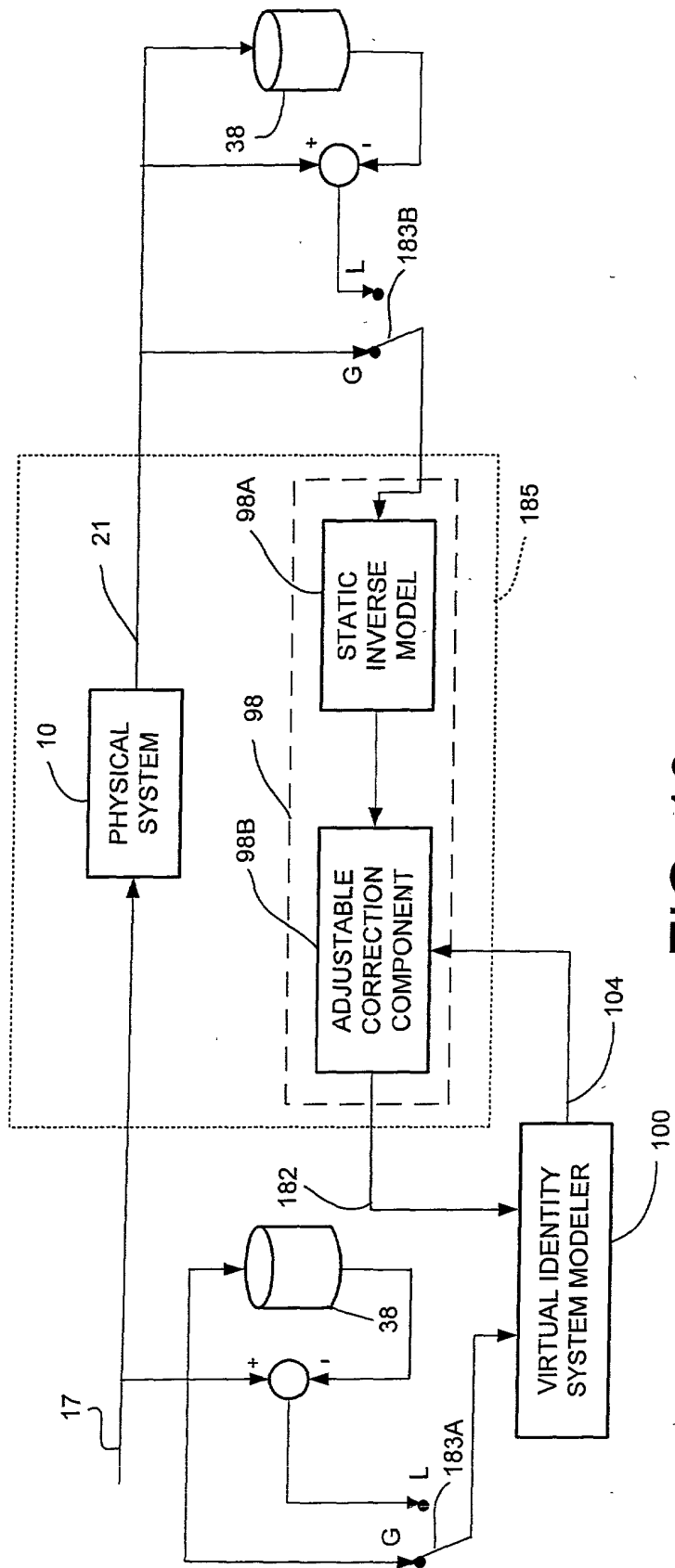


FIG. 10

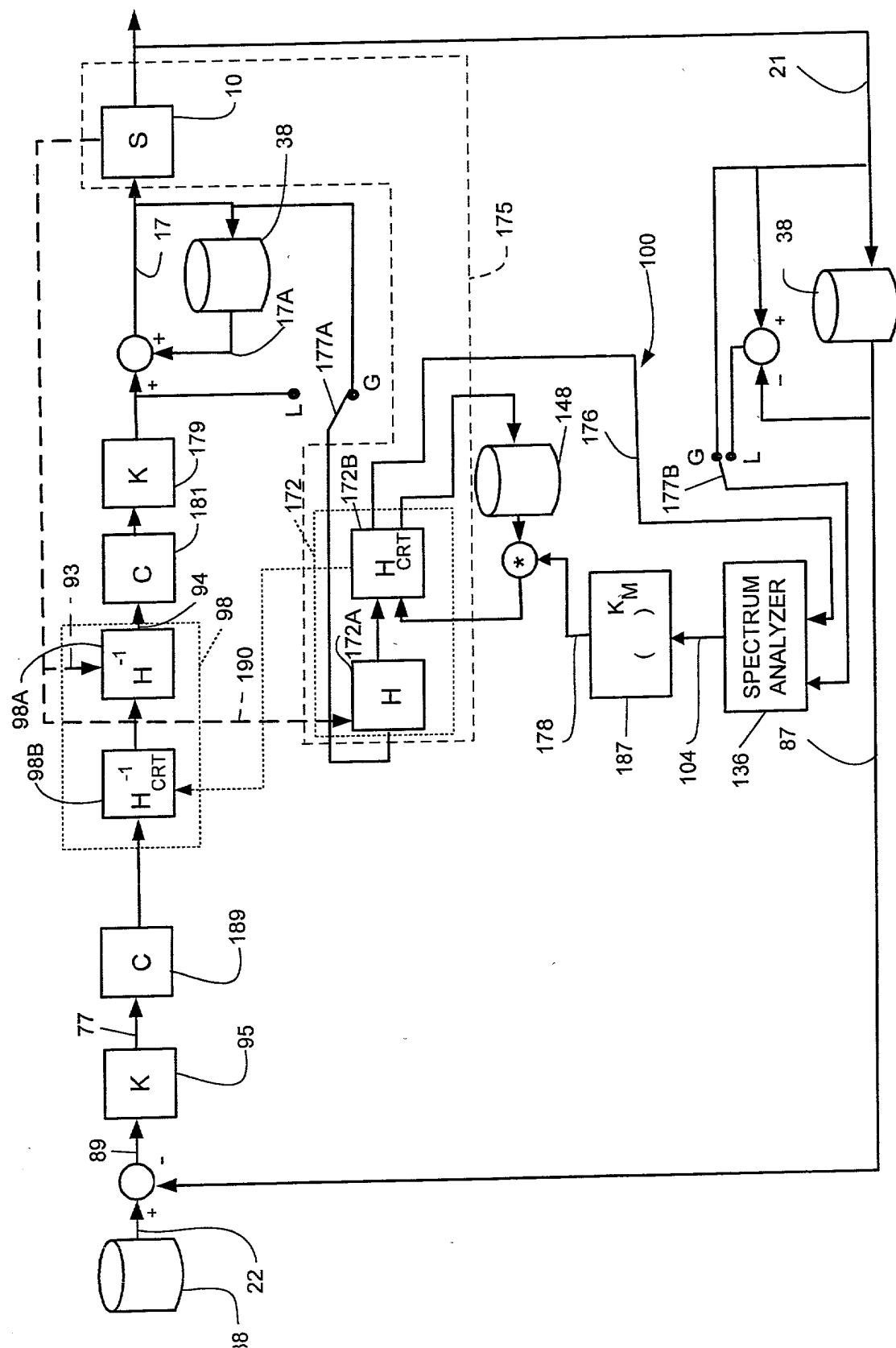


FIG. 11

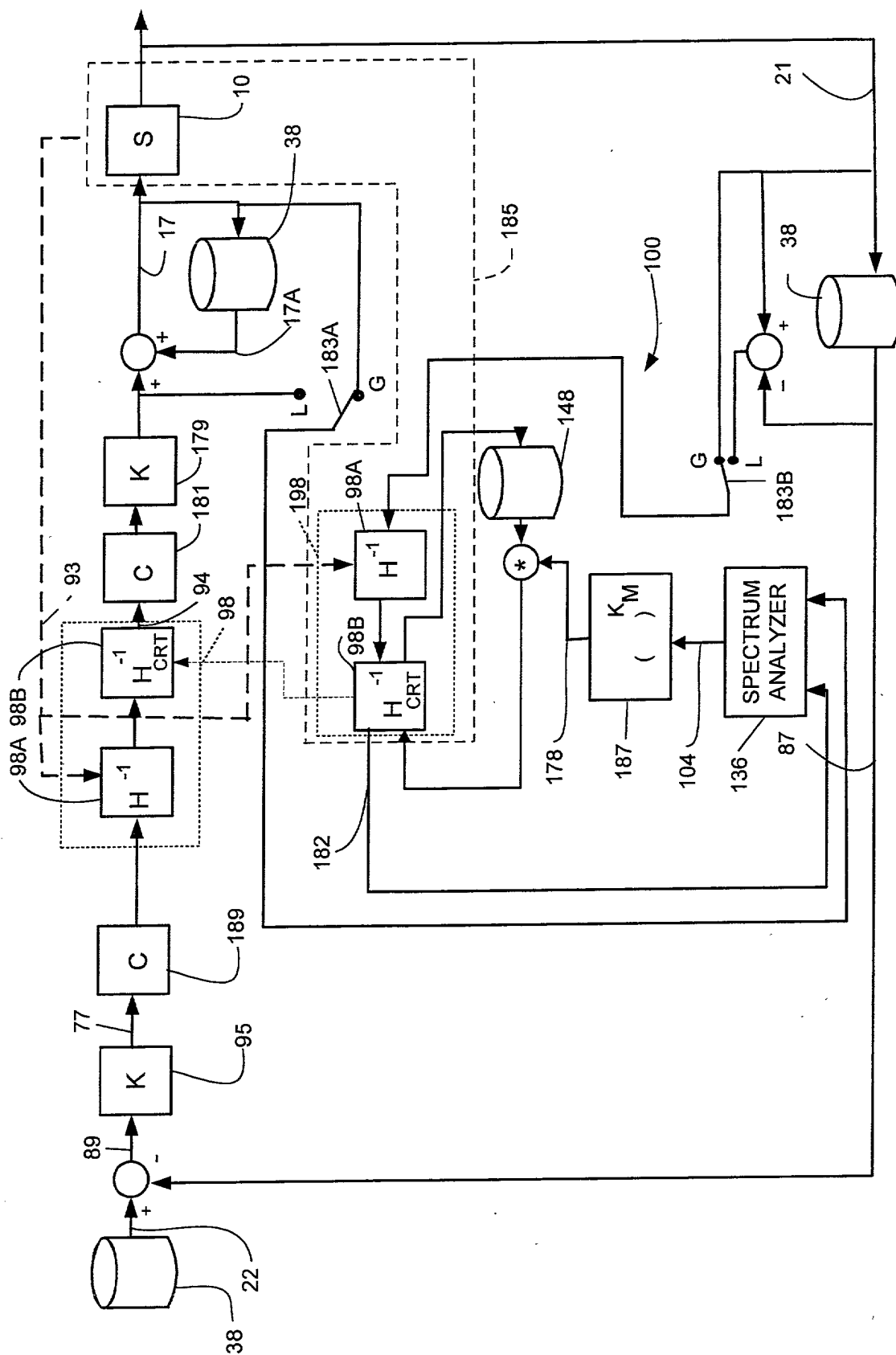


FIG. 12

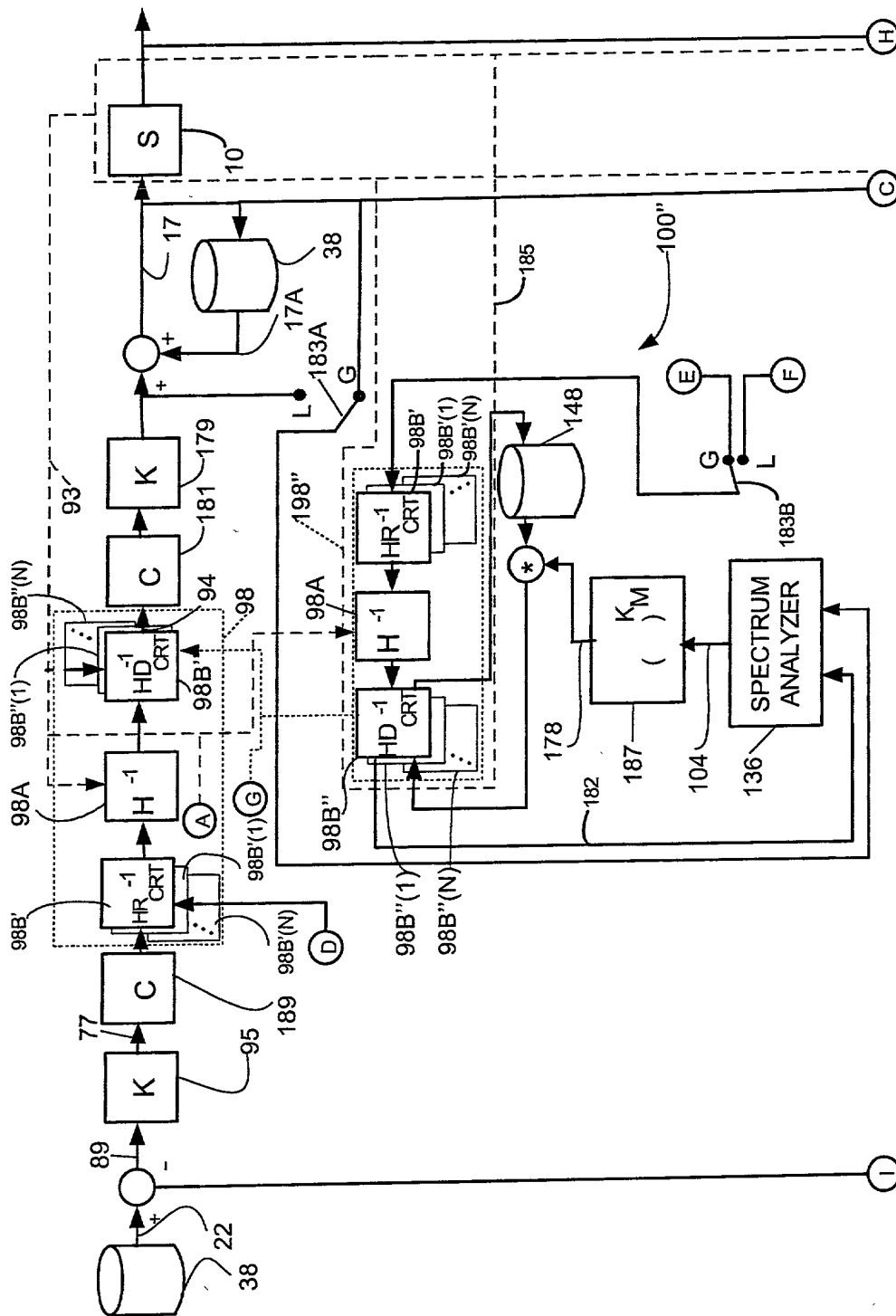


FIG. 13A

The diagram illustrates a system 100 for processing signals from multiple channels. The system includes a central processing unit 175, a spectrum analyzer 136, a memory unit 187, and a storage unit 148. Inputs are labeled A, B, C, D, E, F, G, H, and I. The central unit 175 contains sub-units HD, H, and HR, each with a CRT display. Data flows from inputs through various blocks and a multiplier (*) to a summing junction (+) and a storage unit 21. A feedback loop is shown from the output back to the input.

FIG 13B

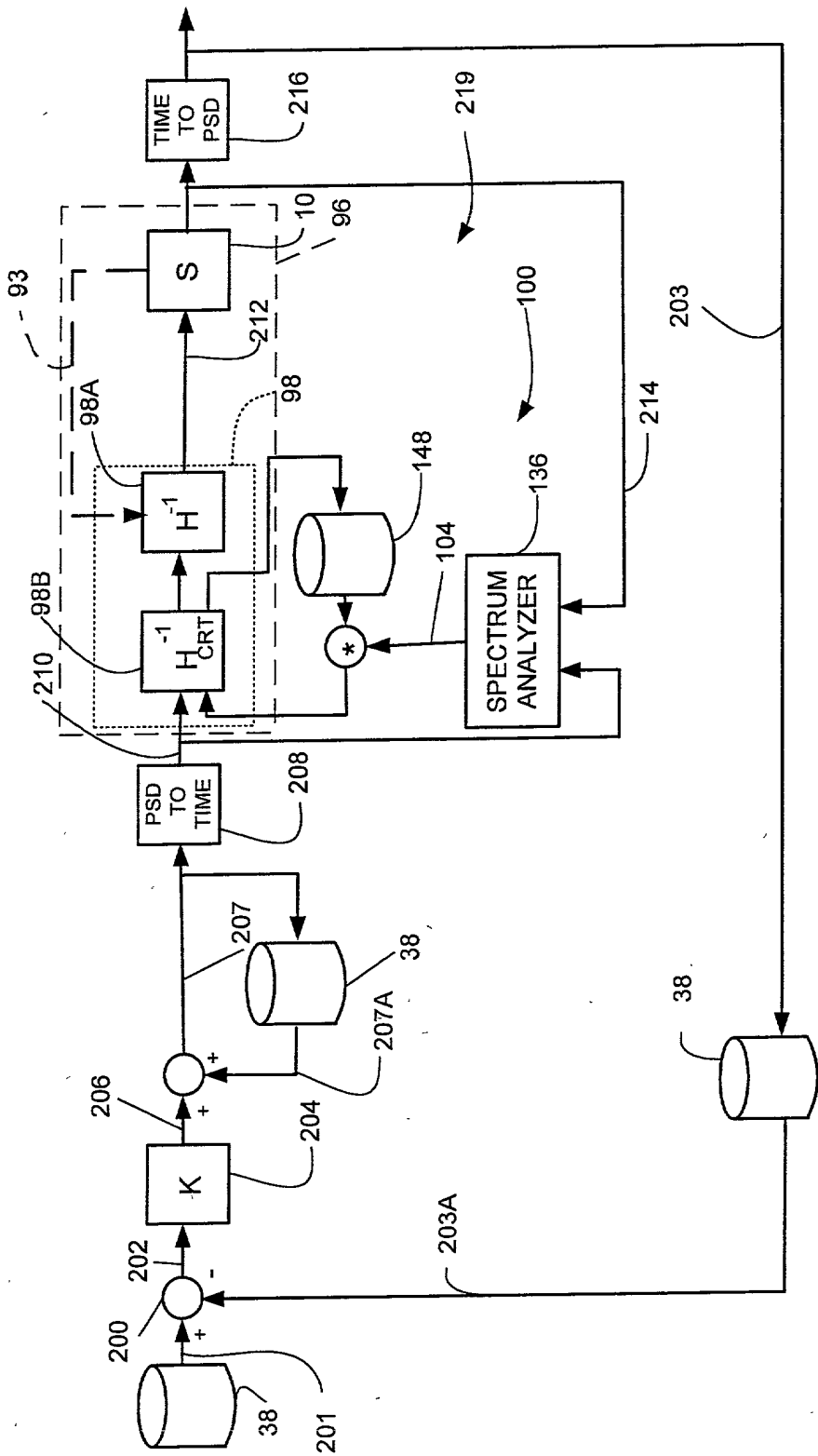


FIG. 14

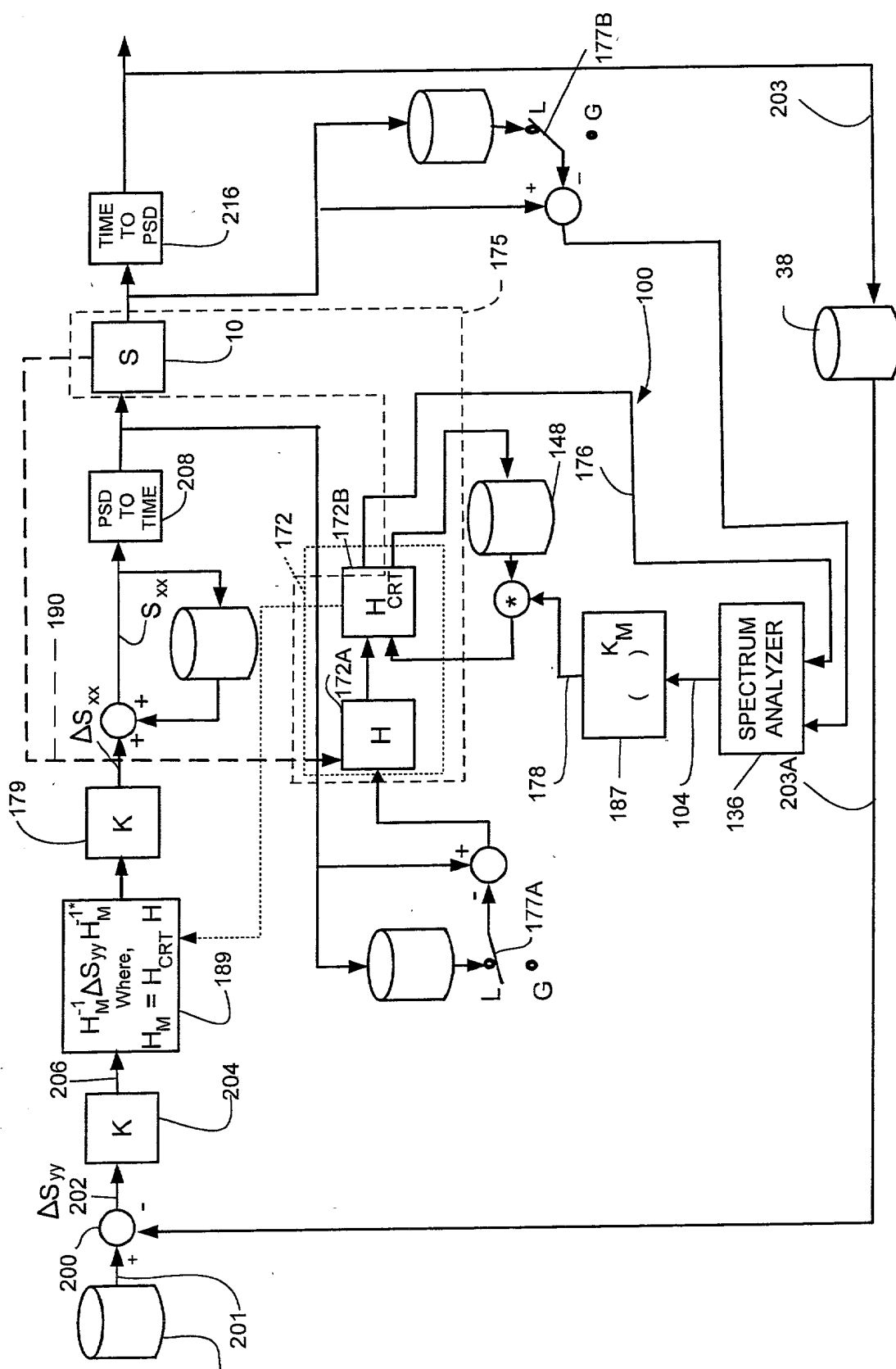


FIG. 15

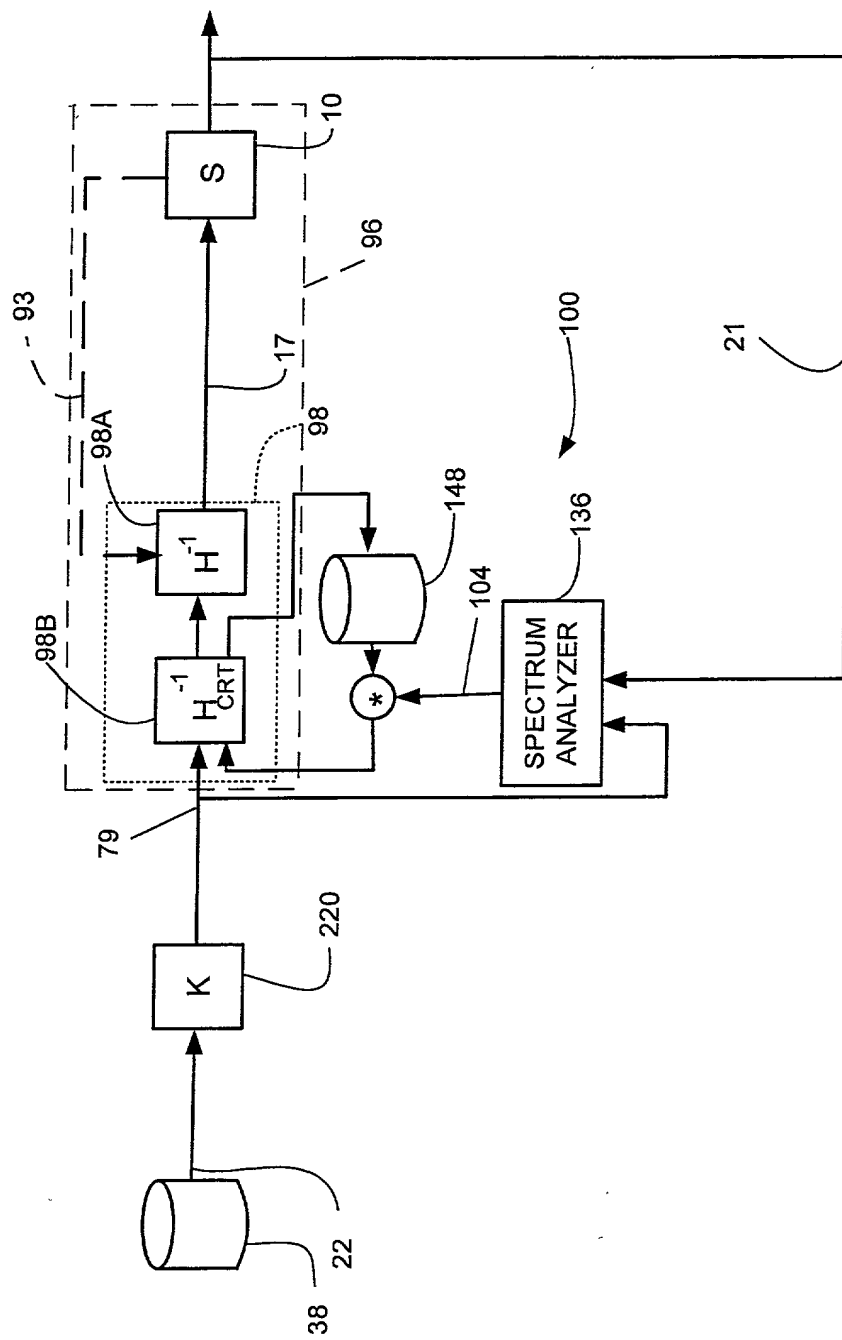


FIG. 16

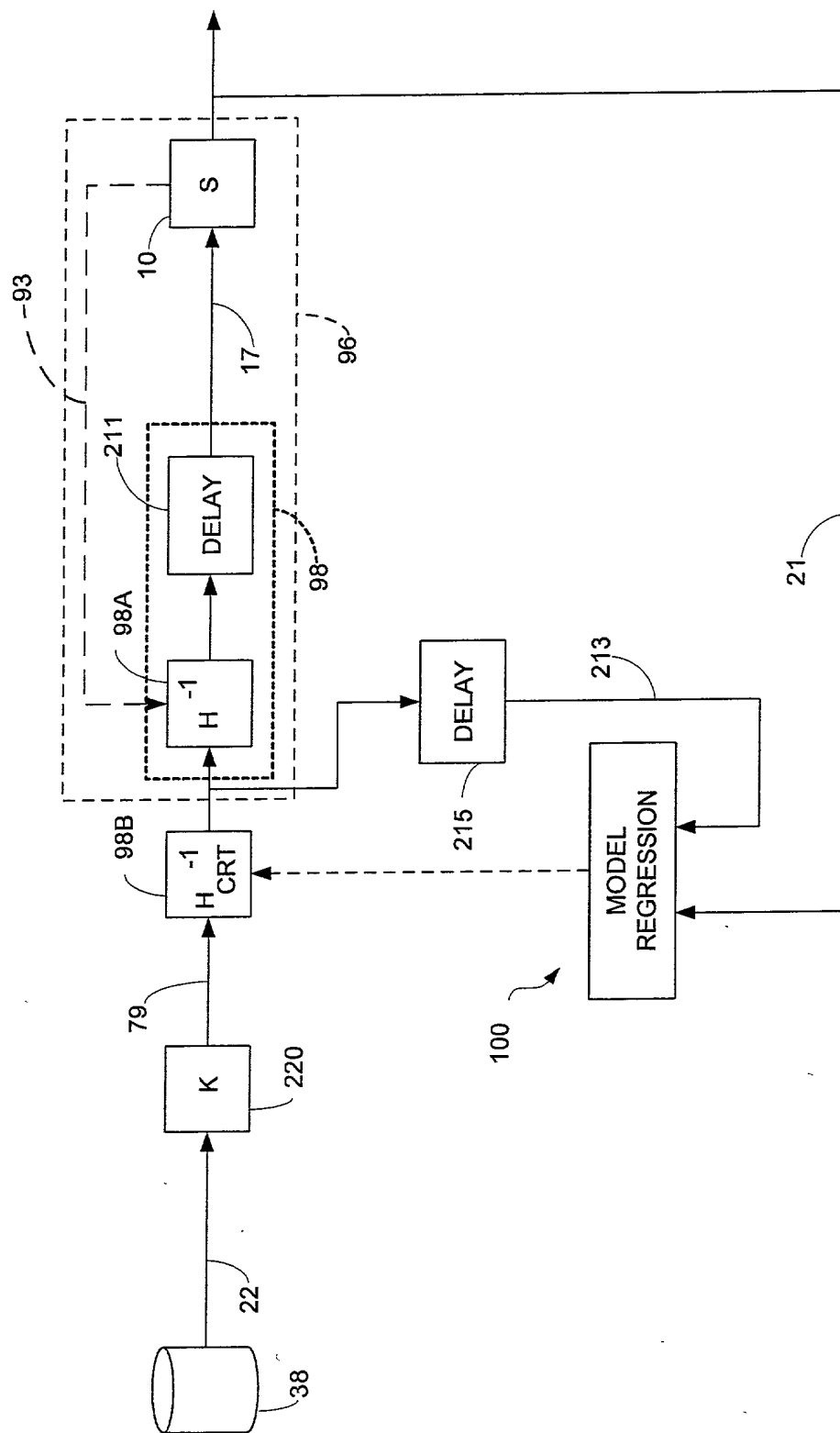


FIG. 17

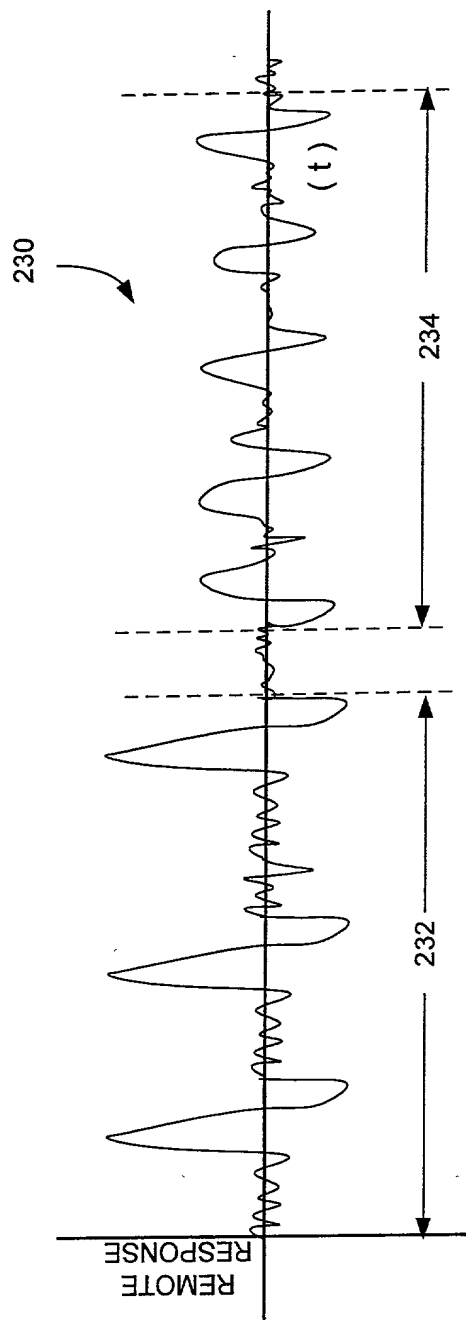


FIG. 18

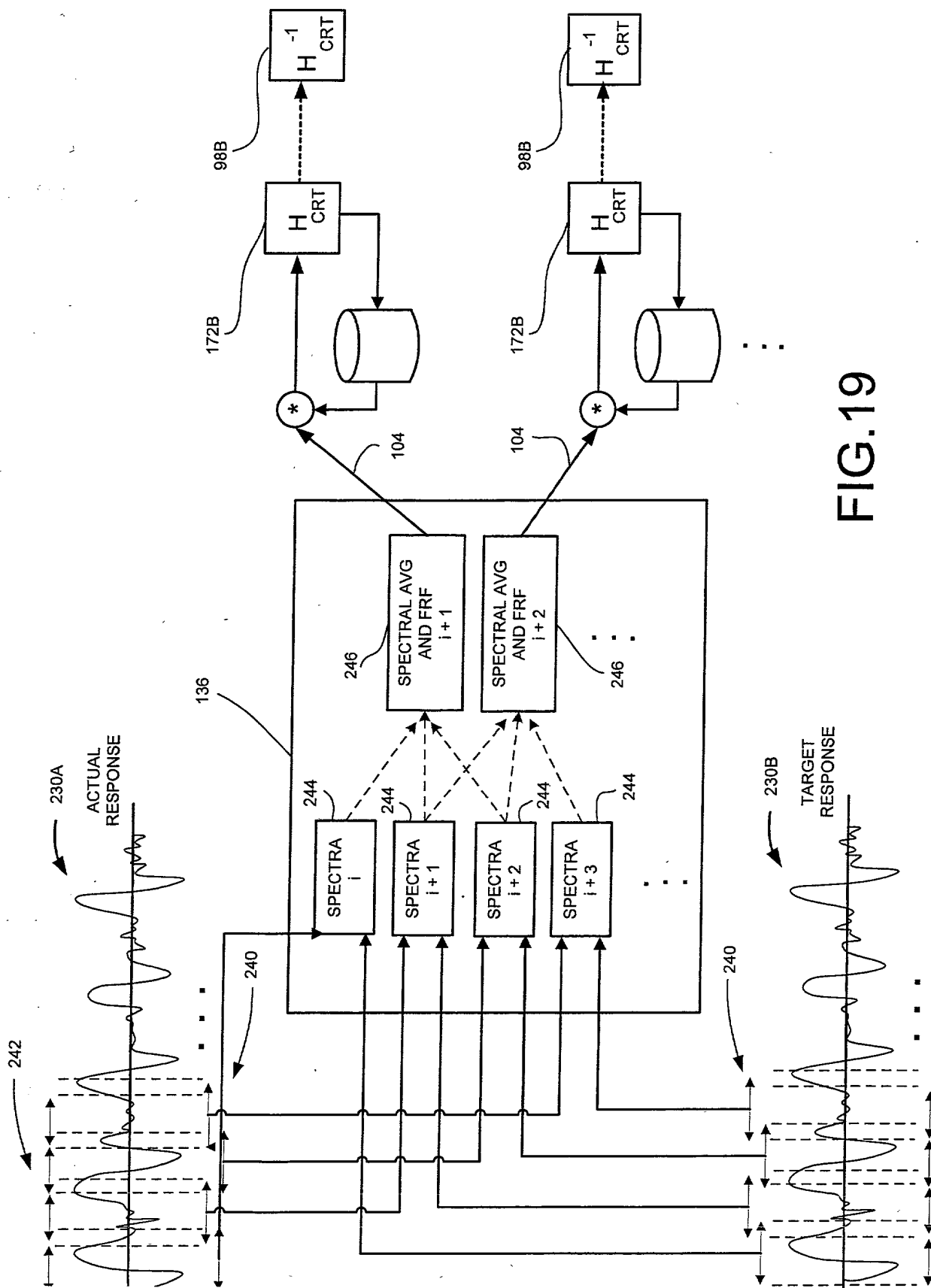


FIG. 19

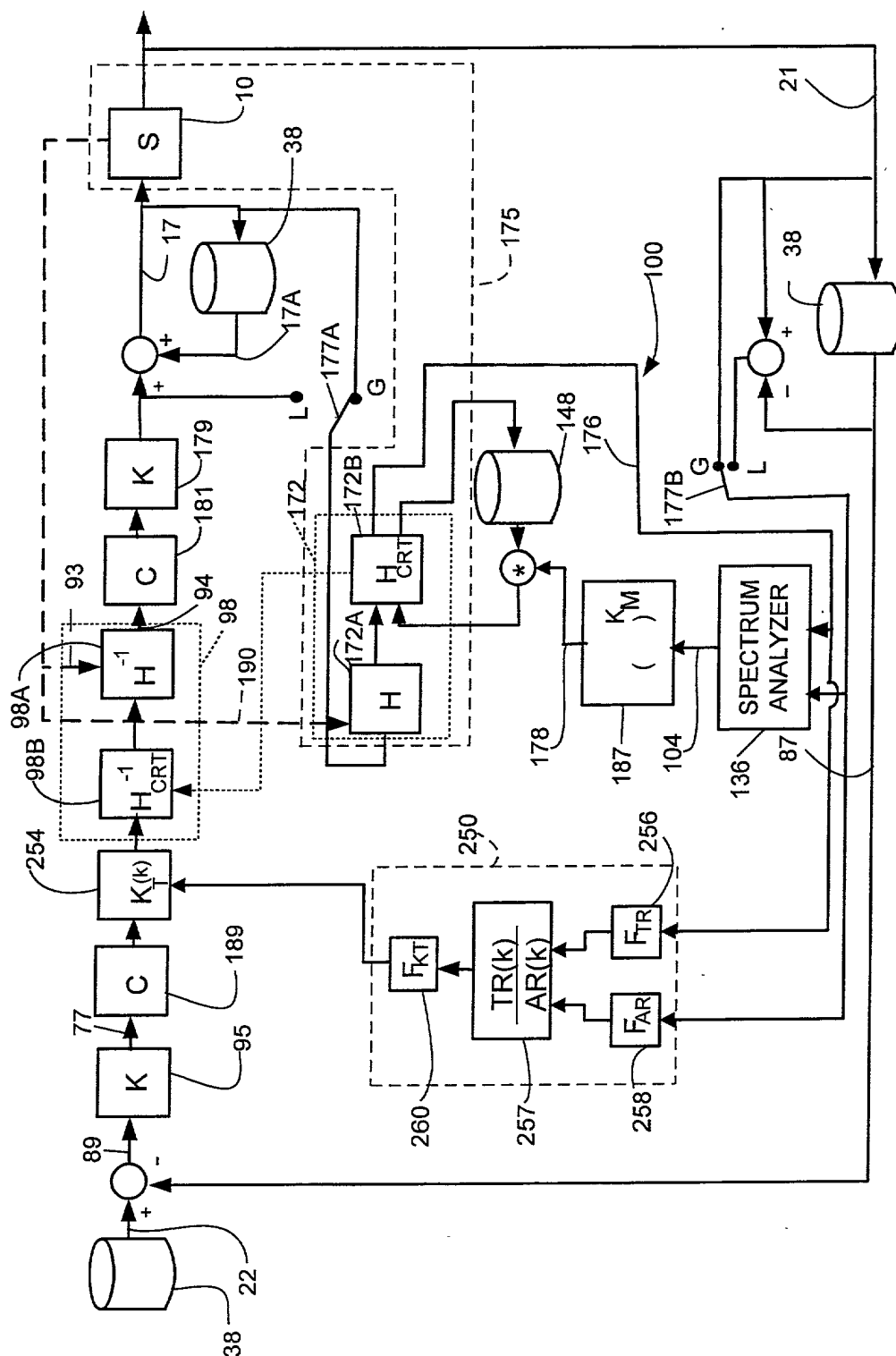


FIG. 20